JEDEC STANDARD

DDR5 Clocked Small Outline Dual Inline Memory Module (CSODIMM) Raw Card C Annex

JESD324-V0-RCC

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(From JEDEC Board Ballot number JCB-24-37, formulated under the cognizance of the JC-45.3 Subcommittee on Unbuffered DRAM Modules, item 2282.13).

1 Scope

This standard, JESD324-V0-RCC, "DDR5 Clocked Small Outline Dual Inline Memory Module (CSODIMM) Raw Card C Annex" defines the design detail of x16, 1 Package Ranks DDR5 CSODIMM with Clock Driver. The common feature of DDR5 CSODIMM such as the connector pinout can be found in the JESD324, DDR5 Clocked Small Outline Dual Inline Memory Module (CSODIMM) Common Specification.

2 DDR5 CSODIMM Design File

Table 1 — DDR5 CSODIMM Design File

Raw Card	Applicable Design File	Applicable BOM
C0	PC5-CSODIMM_RC_C0_R100_20240910.brd	PC5-CSODIMM_RC-C0_R100_20240910_BOM.xlsx
NOTE 1	"Reference" design file updates will be released as needed. This DIMM Annex specification will reflect the most recent design file but may also be updated to reflect clarifications to the Annex only. In these cases, the design file will not be updated.	

3 Module Configuration

Table 2 — Module Configuration

SDRAM			DIMM					
Die Density	Organization	Pkg Type	Maximum Capacity	Organization	# of SRDAM Die on DIMM	# of Package Ranks	# of Address signals Row / Col	MO-337 Variation
16 Gb	1G x 16	SDP	8GB	1G x 32 x 2	4	1	16 / 10	AAxX
24 Gb	1.5G x 16	SDP	12GB	1.5G x 32 x 2	4	1	17 / 10	
32 Gb	2G x16	SDP	16GB	2G x 32 x 2	4	1	17 / 10	

4 SDRAM Configuration

Table 3 — SDRAM Configuration

Raw Card	Supported DRAM Outline (Width x Length) max. (mm)	# of Banks in SDRAM BG / BA	SDRAM Package Type	Package Type	MO-210 Variation
C0	10.3 x 14.1	4/4	106 Ball FBGA 102 Ball FBGA	SDP	AU AT
NOTE 1 SDP is a single die per package. NOTE 2 106ball FBGA has four mechanical support locations with one at each corner					

5 Supported Speeds

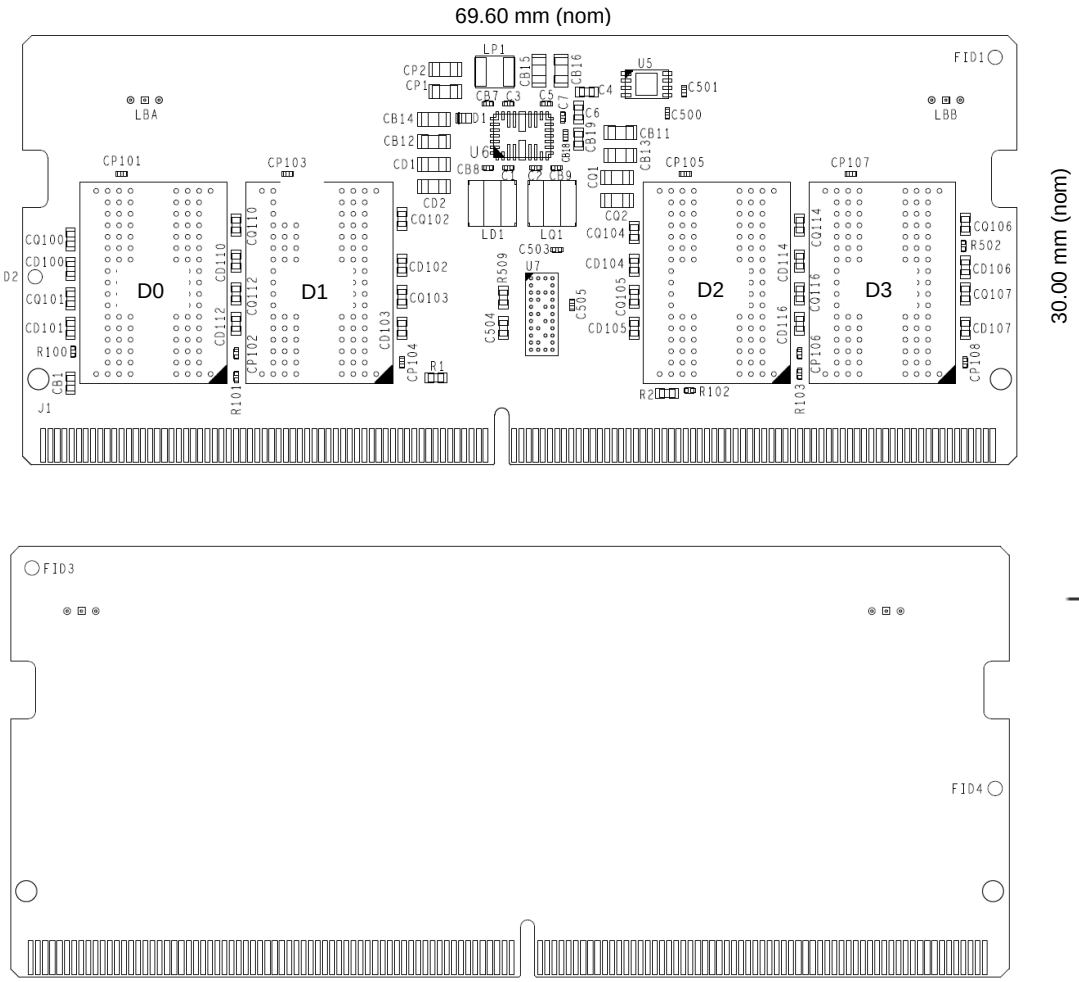
Table 4 — Supported Speeds

Raw Card	Speed	PC5-4400	PC5-4800	PC5-5600	PC5-6400	PC5-7200	PC5-8000	PC5-8800	Notes
C0	DDR5	Y	Y	Y	Y				1,2
NOTE 1 X reflects speed grades approved from previous ballots NOTE 2 Y denotes speed grades being proposed for this most recent ballot									

6 Design Deviations

None.

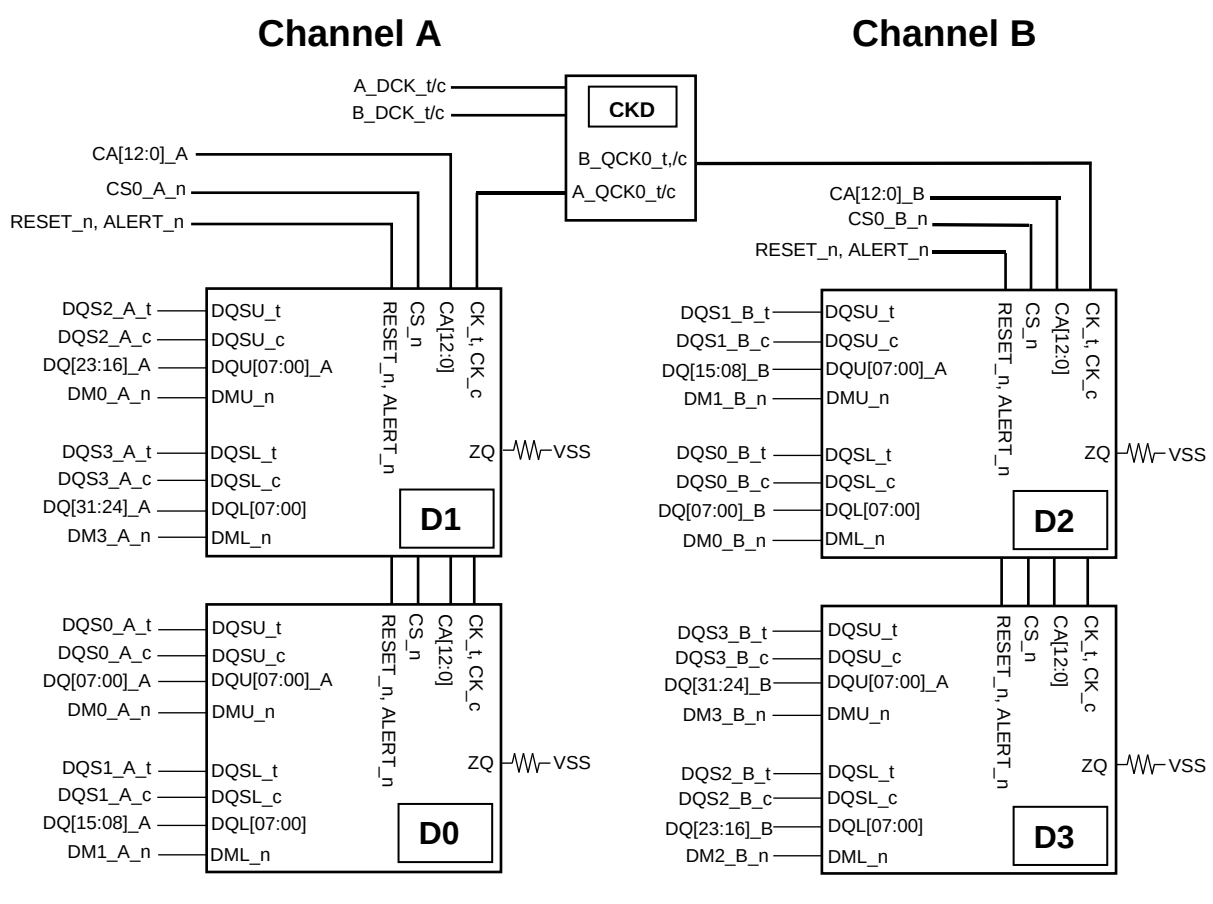
7 General Layout



1. Refer to MO-337 for more detailed information.
2. Variation is AAxX (A Module thickness, x Module height, x plating, X Key Position).
3. Single Sided Assembly

Figure 1 — General Layout

8 Functional Block Diagram



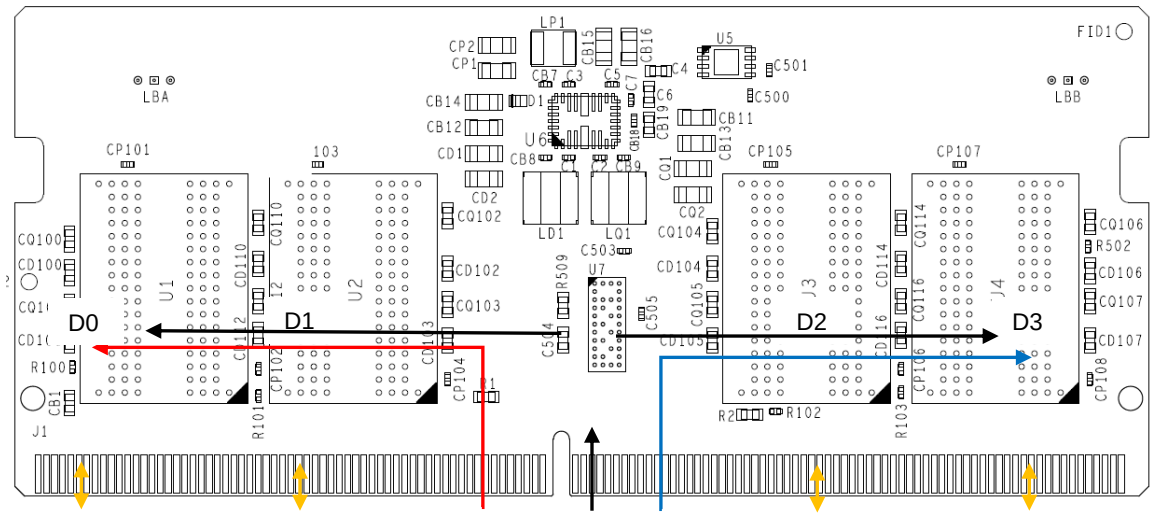
Wiring				
	Channel A		Channel B	
Signal	D0	D1	D2	D3
CA_ODT	VDDQ	VSS	VSS	VDDQ
MIR	VSS	VSS	VSS	VSS
TEN	VSS	VSS	VSS	VSS
CAI	VSS	VSS	VSS	VSS

1. ZQ resistors are 240Ω ± 1%.
2. CS1_[A:B]_n edge pin signals are each terminated with 39Ω ± 5% resistor to VSS.

Figure 2 — X64 DIMM, Populated as One Package Rank of x16 DDR5 SDRAMs (Part 1 of 2)

8 Functional Block Diagram (cont'd)

Wiring



- Ch-A: Address, Command, Control (red)
- Ch-B: Address, Command, Control (blue)
- DCK[B:A][1:0]_t/c and QCK[B:A]0_t/c (black)
- Ch-[A:B]: DQ, Strobe, Mask (16bit lanes) (Gold)

Figure 3 — X64 DIMM, Populated as One Package Rank of x16 DDR5 SDRAMs (Part 2 of 2)

8 Functional Block Diagram (cont'd)

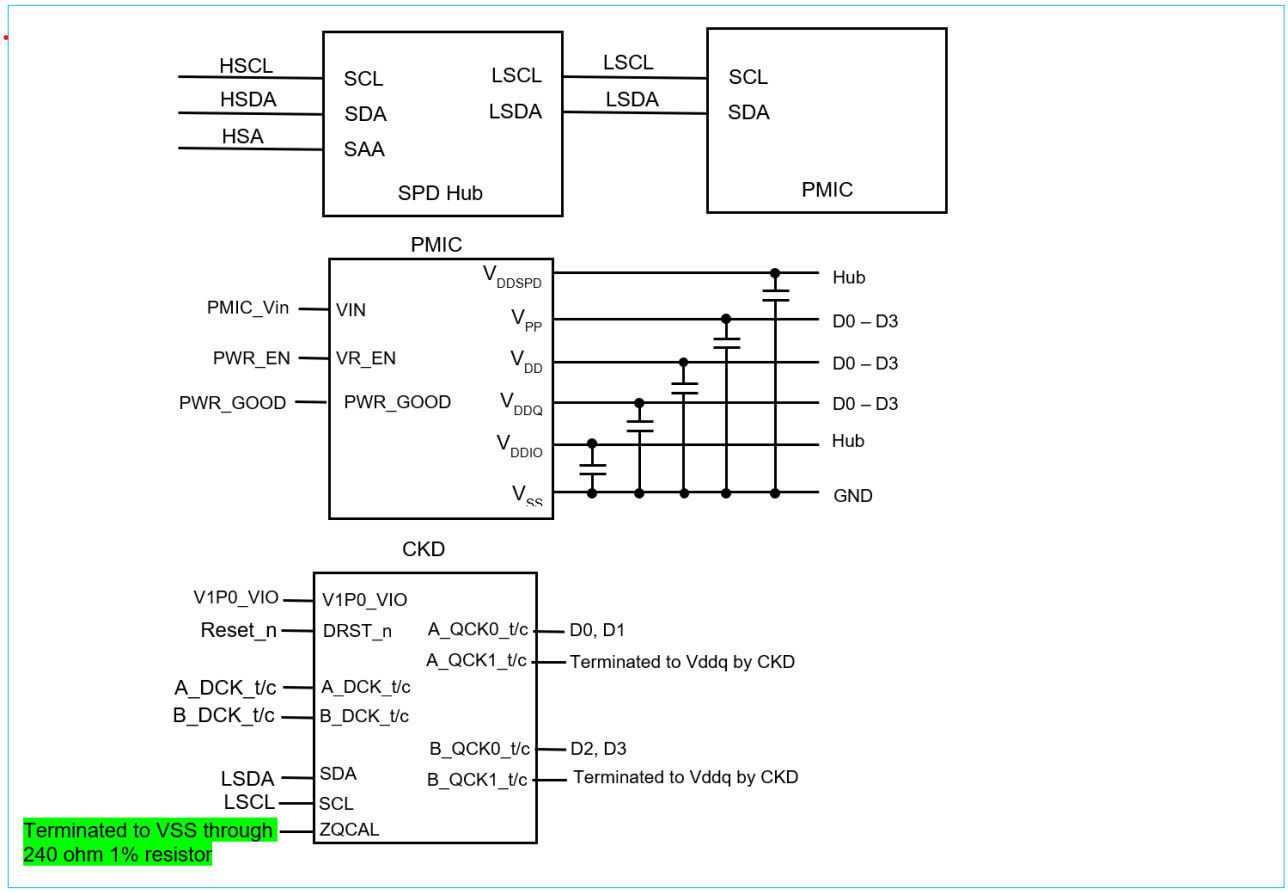


Figure 4 — Functional Block Diagram (Terminated to VSS through 240-ohm 1% Resistor)

9 Sideband Bus Routing

Table 5 — Trace Lengths for Host and Local Signals

Raw Card	Signal	Total Etch Length
C0	HSCL (Gold finger to Hub)	72.0
	HSDA (Gold finger to Hub)	69.7
	HSA (Gold finger to Hub)	69.6
	LSCL (between Hub and PMIC)	8.3
	LSDA (between Hub and PMIC)	8.7
	LSCL (between Hub and CK01)	20.1
	LSDA (between Hub and CK01)	21.8
NOTE 1 All distances are given in (mm).		

10 Clock Net Structure

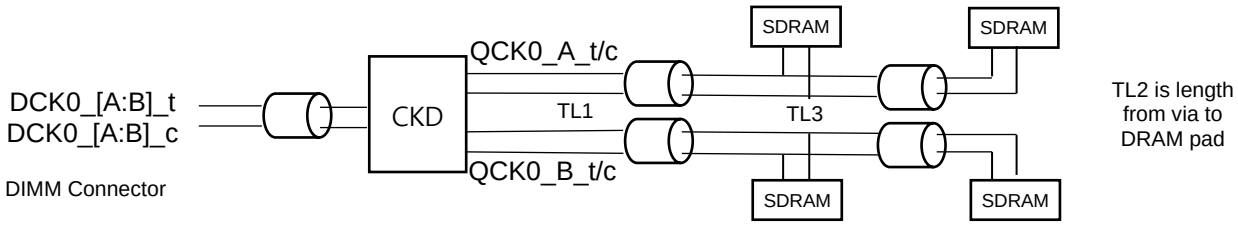


Figure 5 — Net Structure Routing for Clocks - DCK_[1:0]_[B:A]_t/c, QCK0_[B:A]_t/c

Table 6 — Trace Lengths for Clock Net Structures

Raw Card	Signal	TL0 (ms)	TL1 (sl)	TL2 (ms)	TL3 (SL)	Via Travel	Compensated Length 1st SDRAM (or CK01)	Compensated Length 2nd SDRAM
C0	DCK0_A_t	4.42	3.13	0.50		1.02	8.6	
	DCK0_A_c	4.42	3.13	0.50		1.02	8.6	
	DCK0_B_t	4.17	3.53	0.50		1.02	8.8	
	DCK0_B_c	4.17	3.54	0.50		1.02	8.8	
	DCK1_A_t	5.55	8.56	0.50		1.11	15.2	
	DCK1_A_c	5.55	8.56	0.50		1.11	15.2	
	DCK1_B_t	6.05	7.94	0.50		1.11	15.0	
	DCK1_B_c	6.05	7.93	0.50		1.11	15.0	
	QCK0_A_t	0.50	17.92	0.57	13.80	1.02	20.9	34.7
	QCK0_A_c	0.50	17.92	0.57	13.8	1.02	20.9	34.7
	QCK0_B_t	0.50	17.93	0.57	13.82	1.02	20.9	34.8
	QCK0_B_c	0.50	17.92	0.57	13.82	1.02	20.9	34.8

NOTE 1 All distances are given in (mm). Refer to JESD324 for length matching rule.
NOTE 2 The segment lengths are not required to be met.
NOTE 3 _t/c segment lengths of differential pair to be within +/- 0.1 mm
NOTE 4 TL1 segment is MS + SS etch length
NOTE 5 Microstrip sections are converted to equivalent Stripline by dividing by 1.1 for compensation.
NOTE 6 Via travel is compensated as 1 time the z-axis length of the traveled path less outer layer Cu thickness.
NOTE 7 All distances can be adjusted as necessary to align clock with Address.
NOTE 8 Compensated Length 1st SDRAM = (TL1(ms)/1.1+TL1(sl)+TL2/1.1+Via Travel)
NOTE 9 Compensated Length 2nd SDRAM = (Compensated Length 1st SDRAM +TL3)

11 Address and Command Net Structure Routing

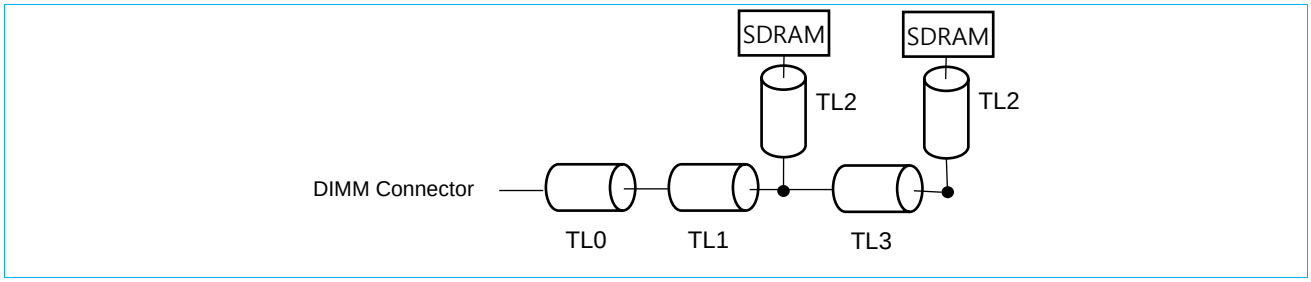


Figure 6 — Net Structure Routing for CA[12:0]_[A:B]

Table 7 — Trace Lengths for Address and Command Net Structures

Raw Card		TL0	Via Travel	TL1	TL3	TL2	Compensation 1st DRAM	Compensation 2nd DRAM
C0	Channel-A CA00A	3.98	0.27	25.14	12.75	0.57	29.55	42.30
	Channel-B CA00B	2.38	1.11	25.78	12.76	0.57	29.56	42.32

NOTE 1 All distances are given in mm. Refer to JESD324 for length matching rule.

NOTE 2 Model for actual SDRAM was used.

NOTE 3 Microstrip sections are converted to equivalent Stripline by dividing by 1.1. Via travel is compensated as 1 time the z-axis length of the traveled path and outer layer Cu thickness is not included.

NOTE 4 All distances can be adjusted within these rules. Address routing lengths between the SDRAMs (TL3) may be adjusted by +/- 3.0 mm relative to the reference design. The segment between the via and the SDRAM ball (TL2) may also be changed as needed.

NOTE 5 Compensated Length 1st SDRAM = ((TL0+TL2) / 1.1 + Via Travel + TL1)

NOTE 6 Compensated Length 2nd SDRAM = (Compensated Length 1st SDRAM +TL3)

12 Control Net Structure Routing

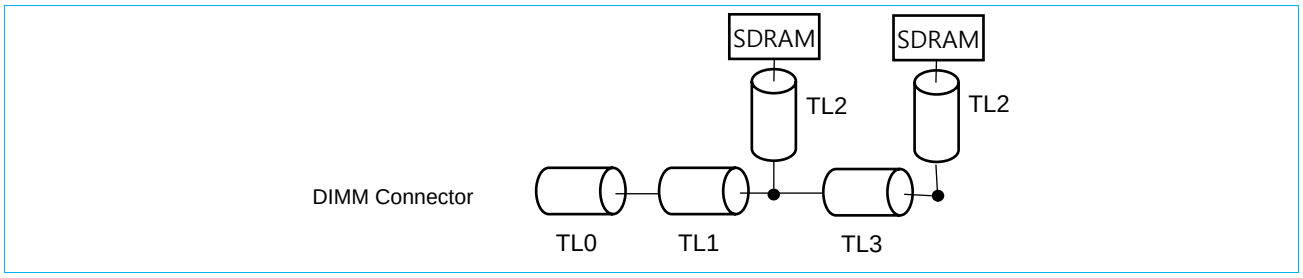


Figure 7 — Net Structure Routing for CS0_[A:B]_n

Table 8 — Trace Lengths for Control Net Structures

Raw Card		TL0	Via Travel	TL1	TL3	TL2	Compensation 1st DRAM	Compensation 2nd DRAM
C0	Channel-A CS0_A_n	2.27	0.27	24.54	12.76	0.95	29.57	42.34
	Channel-B CS0_B_n	3.80	0.27	24.97	12.76	0.95	29.55	42.31

NOTE 1 All distances are given in (mm). JESD324 for length matching rule.

NOTE 2 Microstrip sections are converted to equivalent Stripline by dividing by 1.1. Via travel is compensated as 1 time the Z axis length of the traveled path not including outer layer Cu thickness.

NOTE 3 All distances can be adjusted to keep Chipselect aligned with Clock and Address.

NOTE 4 Compensated Length 1st SDRAM is ((TL0 + TL2) / 1.1 + Via Travel + TL1)

NOTE 5 Compensated Length 2nd SDRAM is (Compensated Length 1st SDRAM + TL3)

13 Data Net Structure Routing - DQ, DQS_t, DQS_c, DM_n

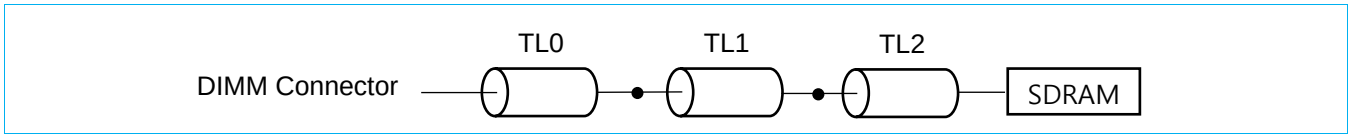


Figure 8 — Net Structure Routing for DQ[31:0]_[A:B], DQS[4:0]_[A:B]_t, DQS[4:0]_[A:B]_c, DM[4:0]_[A:B]_n

Table 9 — Trace Lengths for DQS[7:0]_t, DQS[7:0]_c, DQ[63:0], DM[7:0]_N

Raw Card	Signal Group	Target Signal	TL0	TL1	TL2	Via Travel	Compensated to SDRAM
C0	DQ[07:00]_A	DQ00_A	2.32	11.28	0.57	0.27	14.2
	DM0_A_N	DM00_A	2.24	9.34	1.94	1.02	14.2
	DQS0_A_t DQS0_A_c		4.12	4.93	1.76	1.11	11.4
	DQ[15:08]_A	DQ08_A	3.94	10.73	0.57	0.27	15.1
	DM1_A_N	DM01_A	2.25	10.91	1.10	1.11	15.1
	DQS1_A_t DQS1_A_c		4.12	7.14	1.10	1.02	12.9
	DQ[23:16]_A	DQ16_A	2.25	11.02	0.57	0.27	13.8
	DM2_A_N	DM02_A	2.25	9.01	1.94	1.02	13.8
	DQS2_A_t DQS2_A_c		4.12	6.16	1.76	1.11	12.6
	DQ[31:24]_A	DQ24_A	3.91	10.97	0.57	0.27	15.3
	DM3_A_N	DM03_A	2.25	11.12	1.10	1.11	15.3
	DQS3_A_t DQS3_A_c		4.12	7.13	1.10	1.02	12.9
	DQ[07:00]_B	DQ00_B	2.25	13.14	0.57	0.27	16.0
	DM0_B_N	DM00_B	2.25	12.38	0.57	1.02	16.0
	DQS0_B_t DQS0_B_c		4.12	7.77	1.10	1.11	13.6
	DQ[15:08]_B	DQ08_B	3.85	11.31	0.57	0.27	15.6
	DM1_B_N	DM01_B	2.25	10.86	1.75	1.11	15.6
	DQS1_B_t DQS1_B_c		4.12	8.16	1.76	1.02	14.5
	DQ[23:16]_B	DQ16_B	2.25	13.01	0.57	0.27	15.8
	DM2_B_N	DM02_B	2.25	12.23	0.57	1.02	15.8
	DQS2_B_t DQS2_B_c		4.12	7.71	1.10	1.11	13.6
	DQ[31:24]_B	DQ24_B	3.92	10.86	0.57	0.27	15.2
	DM3_B_N	DM03_B	2.25	10.46	1.75	1.11	15.2
	DQS3_B_t DQS3_B_c		4.12	6.84	1.76	1.02	13.2

NOTE 1 All distances are given in (mm). Refer to JESD324 for length matching rule.

NOTE 2 MS (Microstrip) sections are converted to equivalent SL (Stripline) by dividing by 1.1. Any imbalance in vias is compensated as 1 time the Z axis length of the traveled path not including outer layer Cu thickness.

NOTE 3 Compensated length for DQ and DM bits in a byte lane is +/- 1.0 mm tolerance.

NOTE 4 Compensated length is ((TL0+TL2) / 1.1 + Via Travel +TL1)

14 ALERT_n and RESET_n Net Structure Routing

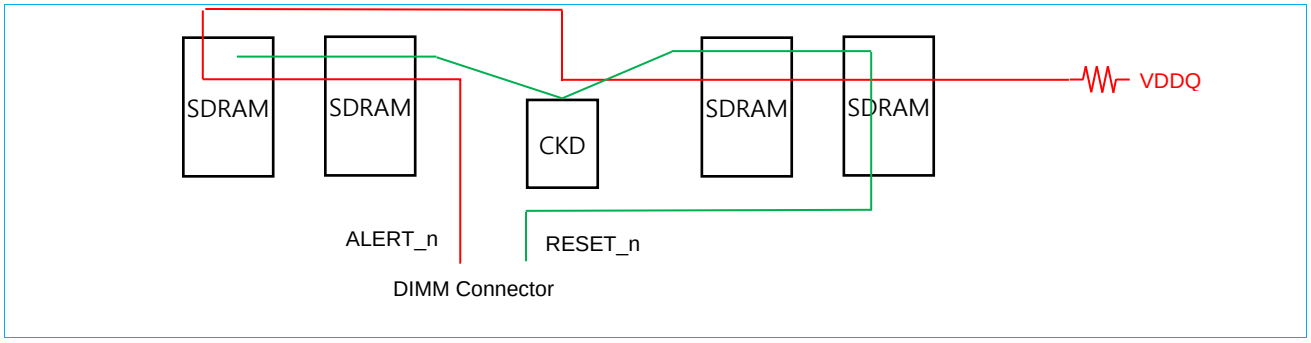


Figure 9 — Net Structure Routing for ALERT_n and RESET_n

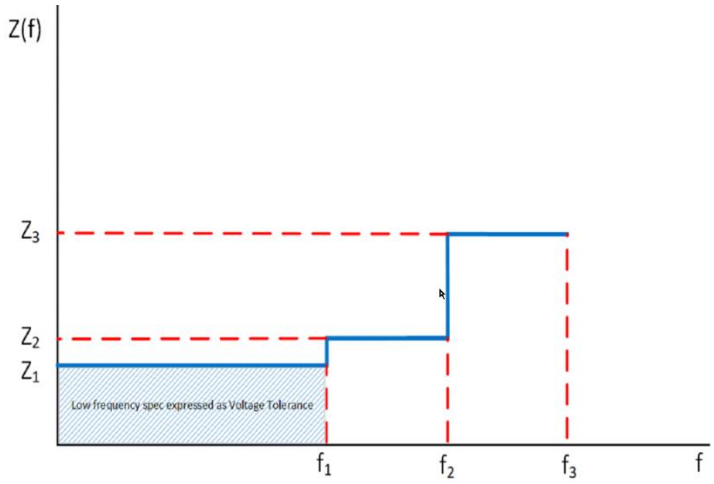
Table 10 — Trace Lengths for ALERT_n and RESET_n Net Structures

Raw Card	Signal	Total Etch Length
C0	ALERT_n	79.3 / 86.4 (without and with TL2 stub)
	RESET_n	94.9 / 101.1 (without and with TL2 stub)

NOTE 1 All distances are given in mm. Length matching is not required but topology must be maintained.
NOTE 2 ALERT_n terminating resistor is 47 +/- 5% ohms.

15 DIMM Impedance Profile

Applies to VDD, VDDQ and VPP voltage rails for this raw card.
Frequency ranges f1, f2, f3 are defined as: f1 ≤ 2 MHz; f2 = 10 MHz; f3 = 20 MHz



NOTE 1 Z(f) targets for each frequency range (Z_1, Z_2, Z_3).

NOTE 2 Z_x is expressed as voltage tolerance based on DRAM input supply tolerances (-3%, +6%)

Figure 10 — DIMM Impedance Profile

Table 11 — Voltage Operating Conditions

Raw Card C0		Voltage Spec Freq: DC to 2 MHz				Z(f) Spec Freq: 2 to 10 MHz		Z(f) Spec Freq: 10 to 20 MHz		Notes
DRAM	Symbol	Minimum (-3%)	Typical	Maximum (+6%)	Unit	Zmax	Unit	Zmax	Unit	
Core Power	VPP	1.746	1.8	1.908	V	25	mOhm	50	mOhm	
Supply voltage	VDDQ	1.067	1.1	1.166	V	15	mOhm	25	mOhm	
Supply Voltage	VDD	1.067	1.1	1.166	V	8	mOhm	15	mOhm	

NOTE 1 VDDQ must be less than or equal to VDD. VDD must be within 66 mV of VDDQ.
NOTE 2 AC parameters are measured separately on VDD and VDDQ.
NOTE 3 DC to 2 MHz voltage range includes all noise at DRAM ball, both DC and AC ripple fluctuations.
NOTE 4 Z(f) is per voltage domain per DRAM device. Per DRAM BGA pin is not required.
NOTE 5 Z(f) does not include the DRAM package and silicon die.

16 DIMM PMIC Configuration

This section defines operating mode, component type, and/or values for DIMM VR.

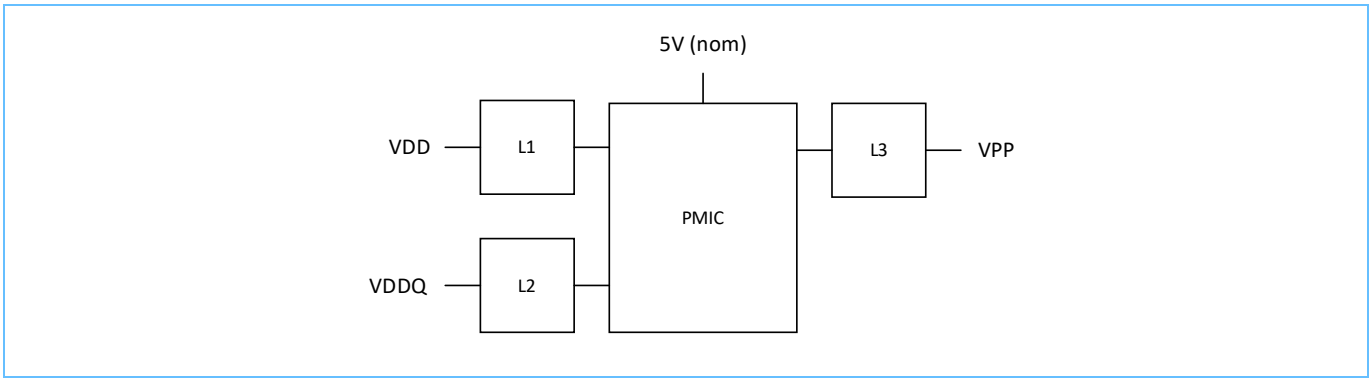


Figure 11 — DIMM PMIC Configuration

Table 12 — RC-C0 VR Settings

PMIC Type	Operation Mode	L1 (VDD)	L2 (VDDQ)	L3 (VPP)	Notes
SDP DRAM package @ 6.4 GT/s					
P5100 Single Phase	Inductor (uH)	0.68 (default) 0.47 (alt)	0.68 (default) 0.47 (alt)	1.0 (default) 1.5 (alt)	
	SWF (kHz)	750 1000 1250	750 1000 1250	750 1000 1250	

NOTE 1 Number of PMIC output capacitor can be determined by DIMM vendors.
NOTE 2 DIMM vendors may optimize SWF and inductor to optimize product.

DIMM PMIC Power Up and Power Down Sequencing and Soft Stop Time

Refer to JESD324 for requirements.

17 Function Control Word Programming

The Register is configured through Register Control Words (RCW).

Some of the Control Words are module PCB design specific and must be programmed the same way for all systems. These are the Control Words that are defined in Table 13

Table 13 — RC C0 – SPD Programming

SPD Byte	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
229	0	0	0	0	0	0	1	0	02	Vin_bulk – TVS
230	0	0	0	0	1	1	1	1	0F	Module Nominal Height (30.00)
231[1]	0	0	0	0	0	0	0	1	01	Module Thickness (Front 1~2 mm / Back < 1 mm)
232	0	0	0	0	0	0	1	0	02	Reference Raw Card Used – C0
233[1]	1	0	0	0	0	0	0	1	81	Temperature Grade - XT, No Heat Spreader, Row-1
234	0	0	0	0	0	0	0	0	00	Module Organization – 1Rx16
235	0	0	1	0	0	0	1	0	22	2 Channels, 0-bit ECC, 32 bit Channel Bus Width
244[1]	1	0	1	0	0	0	0	0	A0	CKD-RW00: CKD Configuration – QCK0's only enabled
245[1]	0	1	0	1	0	1	0	1	55	CKD-RW02 QCK Driver Characteristics - Moderate
246[1]	0	0	0	0	0	0	0	0	00	CKD-RW03: QCK Output Diff Slew Rate - Moderate

NOTE 1 DIMM vendor has option to update these bytes to optimize product

18 Electrically Induced Physical Damage (EIPD) Protection

Protection is provided to the Vin_bulk rail with a discrete Transient Voltage Suppressor TVS.

The Vin_bulk TVS will be an 0402 (1006 metric) footprint in artwork. The TVS for this raw card is placed near the PMIC. The DIMM supplier selects if the TVS is to be uni-directional or bi-directional. The TVS electrical characteristics to be VRWM minimum of 5.5 V and VRWM nominal of 6 V. Other characteristics to be determined by the DIMM supplier.

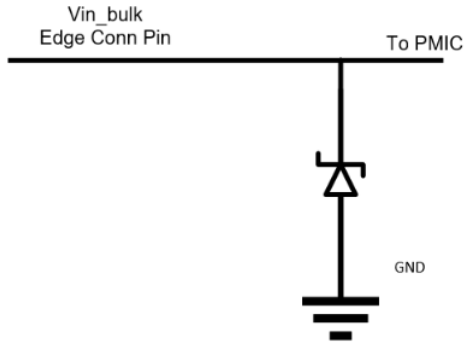


Figure 12 — Electrically Induced Physical Damage (EIPD) Protection

19 Loading and Test Points

Table 14 — Loading

Signal Name	Wiring	Loads per signal
DCK[1:0]_[B:A]_t/c	DIMM edge finger pin to CK01 pin	1
QCK0_[B:A]_t/c	CK01 pin to SDRAM pin	2
CA[12:0]_[A:B]	DIMM edge finger pin to SDRAM pins	2
CS0[A:B]_n	DIMM edge finger pin to SDRAM pins	2
ALERT_n, / RESET_n	DIMM edge finger pin to SDRAM pins	4 / 5
DQx, DQSx_t/c, DMx	DIMM edge finger pin to SDRAM pins	1
HSCL, HSDA, HSA	DIMM edge finger pin to Hub pins	1
LSCL, LSDA	Hub to PMIC and CK01	3
NOTE 1 CS1_[A:B]_n signals are not connected to SDRAM and are terminated to VSS near edge pin fingers. NOTE 2 CK[1:0]_[A:B]_t/c edge connector signals are connected to CK01 pins.		

Table 15 — Test Point Locations

Signal Name	Probe Location
DCK[1:0]_[B:A]_t/c	Via at CK01
QCK0_[B:A]_t/c	Via at SDRAM
CA[12:0]_[A:B]	Via at SDRAM
CS0[A:B]_n	Via at SDRAM
ALERT_n, RESET_n	Via at SDRAM, and CK01 (RESET_n)
DQx, DQSx_t/c, DMx	Via at SDRAM
HSCL, HSDA, HSA	Pin of Hub
LSCL, LSDA	Pin of Hub, pin of PMIC, via at CK01
LBDQ, LBDQS	Test Point
NOTE 1 Refer to the registration package for location of via and pin for probing signals of interest.	

20 Cross Section Recommendations

PCBs should contain solid ground plane and power plane layers as far as possible. Any exceptions to design rules have been identified in the front of this annex

Table 16 — PCB Fabrication Table

Layer	Layer Description	Single-ended Impedance		Differential Impedance		Copper (oz)	Layer Thickness (µm)
		Trace Width (mm)	Impedance Target (ohm)	Width/ Space	Impedance Target (Ohm)		
1	DCK			0.145/ 0.100	70±10%	0.3 + Plating	45
	Others[3]	0.100	50±10%				
	DQ, Str & Addr (unloaded)	0.150	40±10%				
	Dielectric						60
2	GND					0.5	15
	Dielectric						60
3	Address (loaded)	0.065	55±10%			0.5	15
	Other[3]	0.080	50±10%				
	DQ, Str & Addr (unloaded)	0.125	40±10%				
	Dielectric						360
4	Other[3]	0.085	50±10%			0.5	15
	DQ	0.130	40±10%				
	QClock	0.265	25±4 ohms	0.129/ 0.100	70±10%		
	Dielectric						60
5	GND					0.5	15
	Dielectric						360
6	Address (loaded)	0.065	55±10%			0.5	15
	Other[3]	0.080	50±10%				
	DQ, Str & Addr (unloaded)	0.125	40±10%	0.130/ 0.100	70±10%		
	Dielectric						60
7	GND					0.5	15
	Dielectric						60
8	DQ, Strobe & Address (unloaded)	0.150	40±10%			0.3 + Plating	45
	(Unused) Clock, Other[3]	0.100	50±10%	0.145/ 0.100	70±10%		
						Thickness	1200

NOTE 1 The recommended construction and impedance can be found in the PCB Fabrication Table. The values in the table were used in the simulations during development, and in the initial DIMM used to verify operation. Deviations should be kept to a minimum.

NOTE 2 Clock and Strobe differential impedance is the result of single ended impedance with spacing in design.

NOTE 3 “Other” refers to signals inclusive of – ALERT_n, RESET_n, Loopback, and Sideband

NOTE 4 QCK trace width at CKD is diameter of BGA pad, 0.230 mm

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Standard Improvement Form **JEDEC Standard No. JESD324-V0-RCC**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

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3103 10th Street North
Suite 240S
Arlington, VA 22201

Email: angies@jedec.org

1. I recommend changes to the following:

☐ Requirement, clause _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

_____

_____

_____

_____

Submitted by

Name: _____ Phone: _____

Company: _____ E-mail: _____

Address: _____

City/State/Zip: _____ Date: _____


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